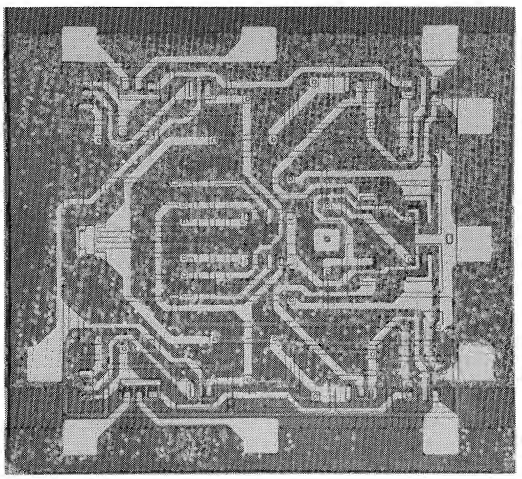
SERIES 15 930
BULLETIN NO. DL-S 668129, FEBRUARY 1966

DIODE-TRANSISTOR LOGIC (DTL) NETWORKS FOR DIGITAL SYSTEMS

application

The series 15 930 networks are designed for use in medium to high-speed digital applications, including data handling, computer and control systems. Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C.



TYPE SN15 931 FLIP-FLOP BAR

features

LOW SYSTEM COST

- **multifunction gates offering low cost per logic function**
- **electrically designed specifically for monolithic integrated-circuit technology**

PERFORMANCE

- **high speed**
- **high d-c noise margins**
- **low power dissipation**
- **good fan-out capability**

EASE OF DESIGN

- **familiar logic configuration (DTL)**
- **single-ended output — dot-OR logic**
- **complete family for design flexibility**
- **single power supply**

description

Series 15 930 is a complete family of diode-transistor logic (DTL) which is most attractive when high performance and low cost per function are necessities to system design.

The basic family consists of NAND gates, an expander, a buffer, a driver and a d-c coupled flip-flop. Dual, triple, and quadruple multi-function-gates are available to minimize system package count.

This line features a unique combination of high speed, high d-c noise margin, and low power dissipation. The single-ended output lends itself readily to performing dot-OR logic thus reducing the number of different type functional blocks in a system.

CONTENTS

†Patented by Texas Instruments Incorporated.

TEXAS INSTRUMENTS
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typical operating characteristics, $T_A = -55°C$ to $125°C$, supply voltage $V_{CC} = 4.5$ v to 5.5 v

Speed: Gate Propagation Delay	25 nsec
Flip-flop Clock Rate	7 Mc
Fan-Out Capability: Standard Gate	8
Flip-flop	7
Buffer	25
Power Gate	27
D-C Margin: At logical 1	500 mv
At logical 0	500 mv
Average Power Dissipation: Per Gate	5 mw
Per Flip-flop	20 mw

design characteristics

Series 15 930 is a complete line of high-speed, high-noise-margin, low-power-dissipation, saturated DTL logic. The circuitry is a modification of the conventional DTL in that it utilizes only one power supply and provides a nonsaturating offset transistor in place of one of the offset diodes.

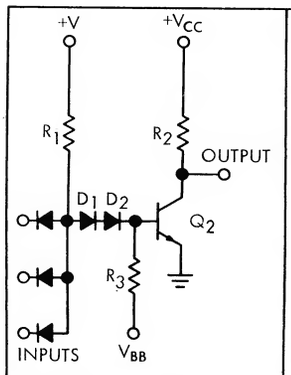


Figure A — Conventional DTL

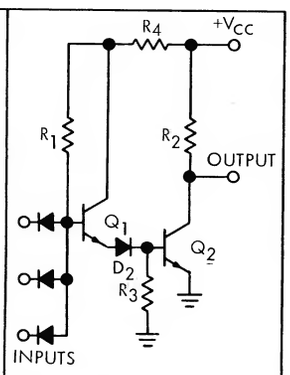


Figure B — Series 15 930

Replacing the offset diode D_1 with transistor Q_1 offers both the manufacturer and the customer a number of advantages:

1. Elimination of the V_{BB} power supply makes one more pin available for multifunction capability, which in turn reduces system package count.

2. Reduction of size of resistor R_3 from 20 kΩ to 5 kΩ invites a substantial reduction in the overall size of the monolithic chip and improves yields. Both of these factors contribute heavily to reducing manufacturing costs.

3. Reduction of turn-off current transients on signal lines is accomplished because the stored charge on the output transistor Q_2 is removed locally by R_3 rather than through diodes D_1 and D_2 onto the input signal lines. These transients are also reduced during switching by the offset transistor Q_1 which operates in the unsaturated mode. This technique eliminates the necessity of producing low-speed, high-stored-charge diodes in the same monolithic bar with fast input diodes.

4. The offset transistor Q_1 provides additional drive current to the output transistor Q_2 without requiring high input currents when the input is in the low state. High input currents would limit fan-out of the driving gates. The additional drive to the output transistor invites the use of a smaller base resistor R_3 and relaxes the h_{FE} requirement of the output transistor thus producing higher manufacturing yields.

In order to drive high-fan-out or high-capacity loads, a buffer is available which has a modified double-ended output. This output has a high-sink-current capability when in the on state and a low-impedance emitter-follower output in the off state.

The d-c coupled flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure C):

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

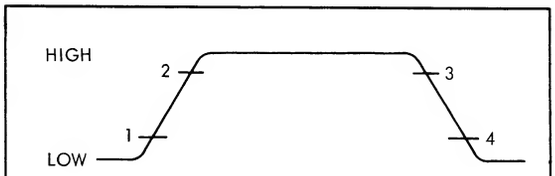
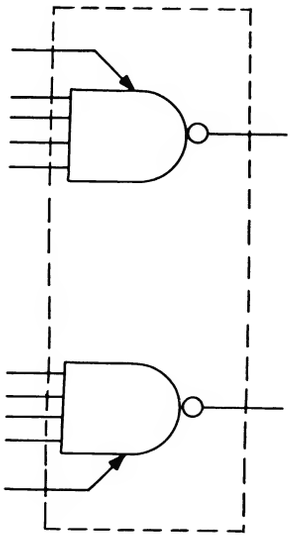


Figure C — Flip-Flop Clock Waveform

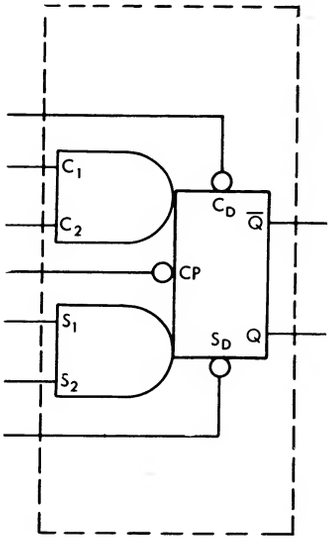
standard line summary

SN15 930 See Page 5



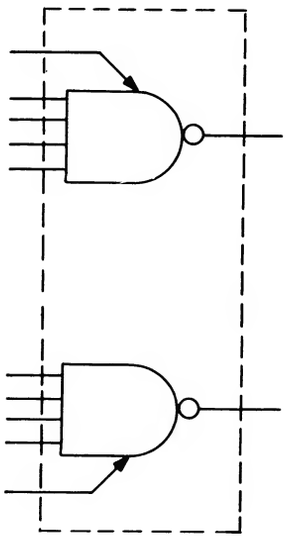
DUAL 4-INPUT
NAND/NOR GATE

SN15 931 See Page 7



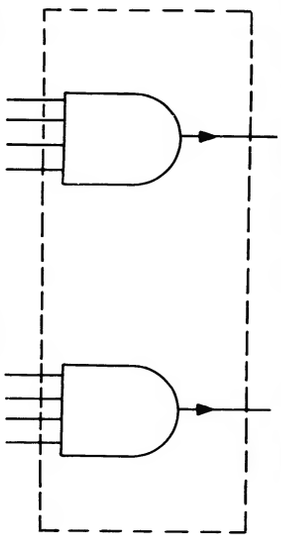
FLIP-FLOP WITH SET AND CLEAR

SN15 932 See Page 9



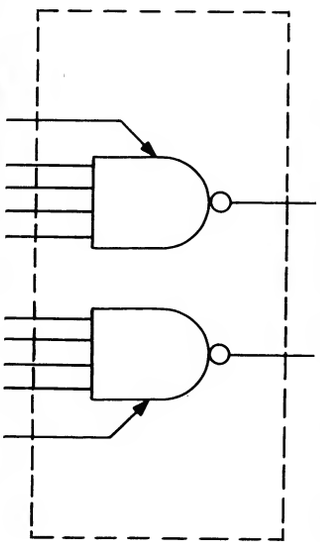
DUAL 4-INPUT
NAND/NOR BUFFER

SN15 933 See Page 11



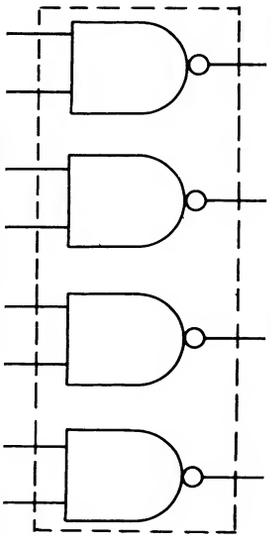
DUAL 4-INPUT EXPANDER

SN15 944 See Page 12



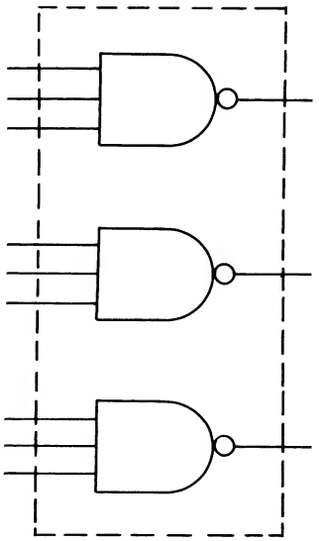
DUAL 4-INPUT
NAND/NOR POWER GATE

SN15 946 See Page 14



QUADRUPLE 2-INPUT
NAND/NOR GATE

SN15 962 See Page 16



TRIPLE 3-INPUT
NAND/NOR GATE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	+8 v
Continuous Output Sink Current (SN15 930, SN15 931, SN15 946 and SN15 962)	30 ma
Continuous Output Sink Current (SN15 932 and SN15 944)	150 ma
Current Out of Input Terminal	−10 ma
Current Into Input Terminal	1 ma
Operating Free-Air Temperature Range (See Note 2)	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies for networks operating at V_{CC} = 5.5 v, all inputs† at 5.5 v, and the following output current:

SN15 930†, SN15 946, SN15 962	12 ma
SN15 931	10.6 ma
SN15 932†	36 ma
SN15 944†	40 ma

†Expander nodes open

logic definition

Series 15 930 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input current requirements

Weighted values of input current requirements reflect worst case conditions for T_A = −55°C to 125°C and V_{CC} = 4.5 v to 5.5 v. Each gate input requires that no more than 1.6 ma flow out of the input at a logical 0 input voltage level; therefore, one input load is 1.6 ma maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS

NETWORK	TYPE	INPUT	NUMBER OF LOADS
GATES AND EXPANDER	SN15 930 SN15 932 SN15 933 SN15 944 SN15 946 SN15 962	Each Input	1
FLIP-FLOP	SN15 931	Each Input (Synchronous or Asynchronous)	⅔
		Clock	2

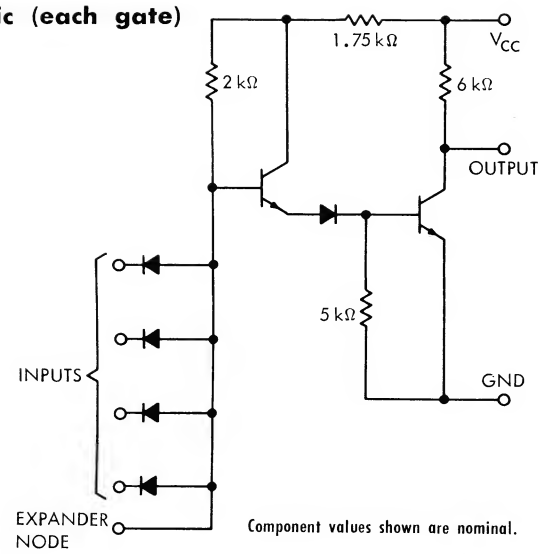
output drive capability

Weighted values of fan-out reflect the ability of an output to sink current (into the ouput terminal) under recommended operating conditions and are specified as positive values. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

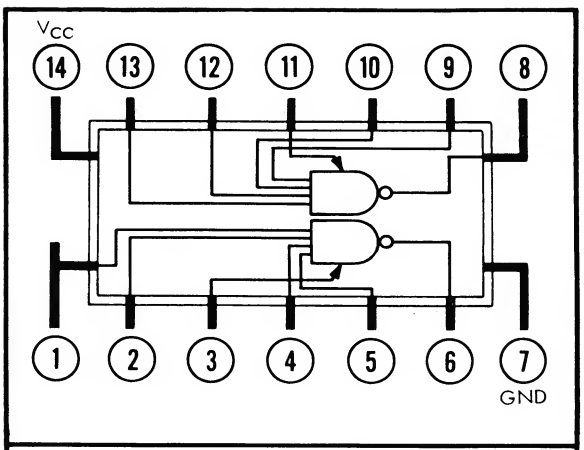
WEIGHTED VALUES OF FAN-OUT

NETWORK	TYPE	OUTPUT	NOMINAL LOADS
FLIP-FLOP	SN15 931	Q or $\overline{Q}$	7
GATES	SN15 930 SN15 946 SN15 962	Each Output	8
BUFFER	SN15 932	Each Output	25
POWER GATE	SN15 944	Each Output	27

schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 v, V_{in} = 1.9 v, I_{sink} = 12 ma, T_A = 25°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 2.1 v, I_{sink} = 11.4 ma, T_A = –55°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 1.7 v, I_{sink} = 10.8 ma, T_A = 125°C		0.45	v
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 v, V_{in} = 1.1 v, I_{load} = 0.12 ma, T_A = 25°C	2.6		v
			V_{CC} = 4.5 v, V_{in} = 1.4 v, I_{load} = 0.12 ma, T_A = –55°C	2.5		v
			V_{CC} = 4.5 v, V_{in} = 0.8 v, I_{load} = 0.12 ma, T_A = 125°C	2.5		v

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage at expander input node, $V_{in(X)}$	3	V_{CC} = 4.5 v, $V_{in(X)}$ = 1.8 v, I_{load} = 0.12 ma, T_A = 25°C	2.6		v
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 25°C and –55°C		-1.6	ma
			V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 125°C		-1.5	ma
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 v, T_A = 25°C		50	μa
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 v, V_{out} = 0, T_A = 25°C	–0.6	–1.34	ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = –55°C		–1.34	ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = 125°C		–1.3	ma
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	V_{CC} = 5 v, T_A = 25°C		6.5	ma
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	V_{CC} = 8 v, T_A = 25°C		5.5	ma

switching characteristics, V_{CC} = 5 v, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$t_{pd(0)}$	Propogation delay time to logical 0 level	27	R_1 = 400 Ω, C_1 = 50 pf	10	30	nsec
$t_{pd(1)}$	Propogation delay time to logical 1 level		R_1 = 3.9 kΩ, C_1 = 30 pf	25	80	nsec

† Expander nodes are open unless otherwise noted.

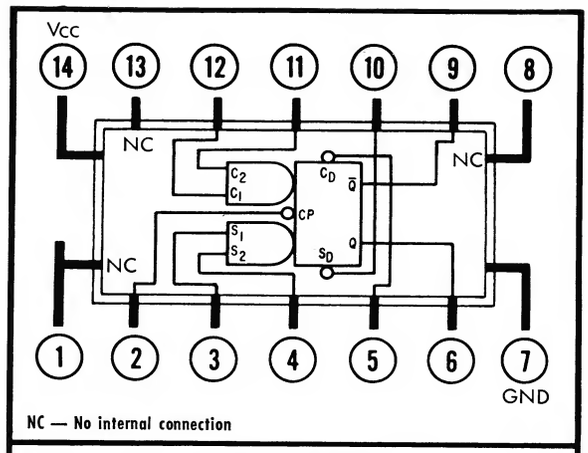
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 v to 5.5 v
Maximum Fan-Out From Each Output 7

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	10	V_{CC} = 4.5 v, $V_{CP(S)}$ = 0.95 v, I_{sink} = 10.6 ma, T_A = 25°C	0.4	v
			V_{CC} = 4.5 v, $V_{CP(S)}$ = 1.1 v, I_{sink} = 10 ma, T_A = –55°C	0.4	v
			V_{CC} = 4.5 v, $V_{CP(S)}$ = 0.75 v, I_{sink} = 9.5 ma, T_A = 125°C	0.45	v
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	11	V_{CC} = 4.5 v, V_1 = 1.9 v, V_2 = 1.1 v, I_{load} = 0.12 ma, T_A = 25°C	2.6	v
			V_{CC} = 4.5 v, V_1 = 2.1 v, V_2 = 1.4 v, I_{load} = 0.12 ma, T_A = –55°C	2.5	v
			V_{CC} = 4.5 v, V_1 = 1.7 v, V_2 = 0.8 v, I_{load} = 0.12 ma, T_A = 125°C	2.5	v
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_{CC} = 4.5 v, V_1 = 1.9 v, V_2 = 1.1 v, I_{load} = 0.12 ma, T_A = 25°C	2.6	v
			V_{CC} = 4.5 v, V_1 = 2.1 v, V_2 = 1.4 v, I_{load} = 0.12 ma, T_A = –55°C	2.5	v
			V_{CC} = 4.5 v, V_1 = 1.7 v, V_2 = 0.8 v, I_{load} = 0.12 ma, T_A = 125°C	2.5	v
$I_{CP(0)}$	Logical 0 level clock-input forward current	13	V_{CC} = 5.5 v, V_{in} = 1.1 v, T_A = 25°C	–3.4	ma
			V_{CC} = 5.5 v, V_{in} = 1.4 v, T_A = –55°C	–3.4	ma
			V_{CC} = 5.5 v, V_{in} = 0.8 v, T_A = 125°C	–3	ma
$I_{CP(1)}$	Logical 1 level clock-input reverse current	14	V_{CC} = 5.5 v, V_{CP} = 4 v, T_A = 25°C and –55°C	20	μa
			V_{CC} = 5.5 v, V_{CP} = 4 v, T_A = 125°C	30	μa

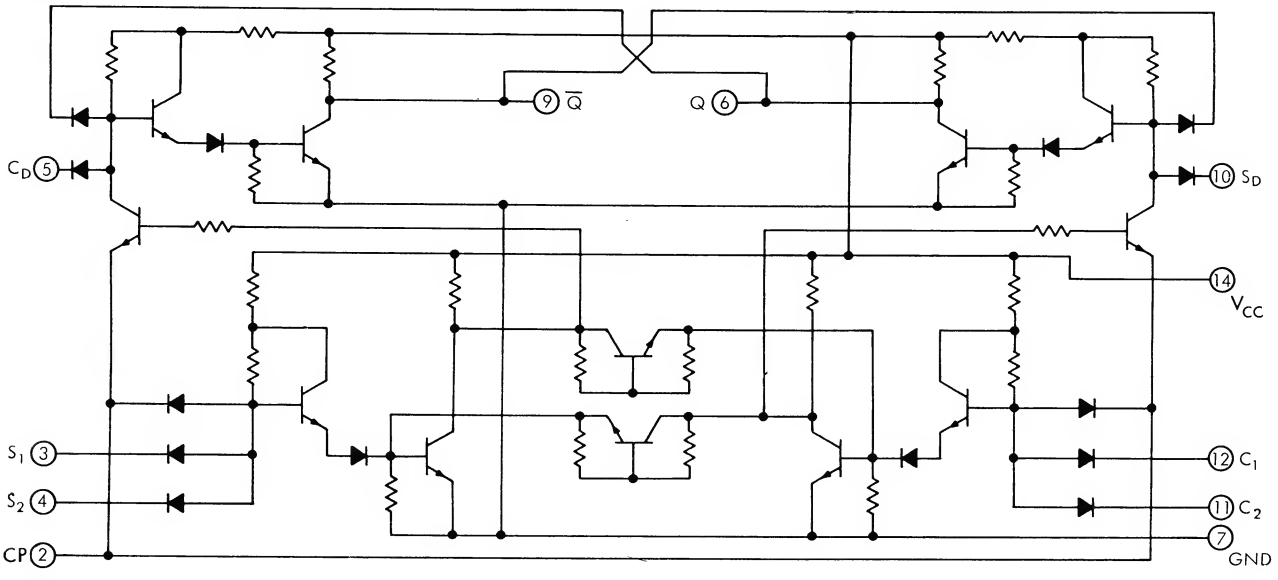
electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	V_{CC} = 5.5v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa
$I_{in(0)}$	Logical 0 level synchronous-input current	16	V_{CC} = 5.5 v, V_{in} = 0, T_A = 25°C and –55°C		–1.07	ma
			V_{CC} = 5.5 v, V_{in} = 0, T_A = 125°C		–1	ma
$I_{in(1)}$	Logical 1 level asynchronous-input current	17	V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa
$I_{in(0)}$	Logical 0 level asynchronous-input current	18	V_{CC} = 5.5 v, V_{in} = 0, T_A = 25°C and –55°C		–1.2	ma
			V_{CC} = 5.5 v, V_{in} = 0, T_A = 125°C		–1.1	ma
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = 5 v, T_A = 25°C		11	ma
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	V_{CC} = 8 v, T_A = 25°C		14.5	ma

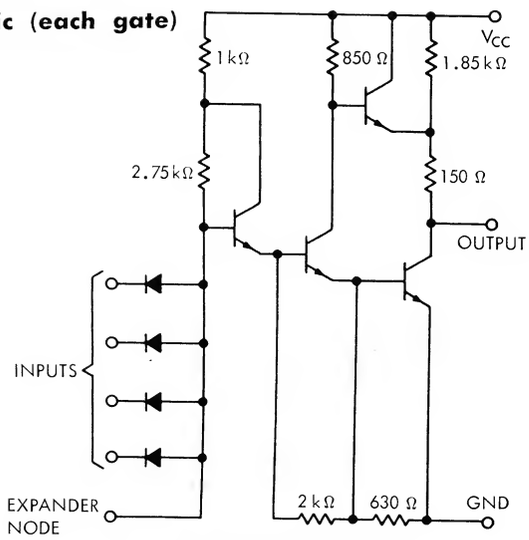
switching characteristics, V_{CC} = 5 v, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	28	R_1 = 400 Ω	35	75	nsec
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 3.9 kΩ	35	75	nsec

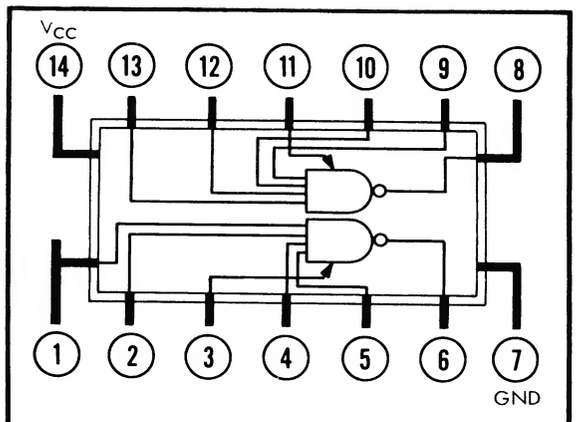
schematic



schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output 25

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 v, V_{in} = 1.9 v, I_{sink} = 36 ma, T_A = 25°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 2.1 v, I_{sink} = 34 ma, T_A = –55°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 1.7 v, I_{sink} = 32 ma, T_A = 125°C		0.45	v
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 v, V_{in} = 1.1 v, I_{load} = 2.5 ma, T_A = 25°C	2.6		v
			V_{CC} = 4.5 v, V_{in} = 1.4 v, I_{load} = 2 ma, T_A = –55°C	2.5		v
			V_{CC} = 4.5 v, V_{in} = 0.8 v, I_{load} = 4 ma, T_A = 125°C	2.5		v

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage input at expander node, $V_{in(X)}$	3	V_{CC} = 4.5 v, $V_{in(X)}$ = 1.8 v, I_{load} = 2.5 ma, T_A = 25°C	2.6		v
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 25°C and –55°C		–1.6	ma
			V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 125°C		–1.5	ma
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 v, T_A = 25°C		50	μa
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 v, V_{out} = 0, T_A = 25°C	–18		ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = 125°C and –55°C	–16		ma
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	V_{CC} = 5 v, T_A = 25°C		26.6	ma
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	V_{CC} = 8 v, T_A = 25°C		6	ma

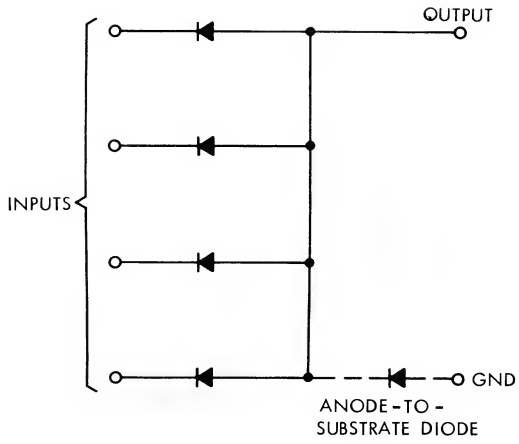
switching characteristics, V_{CC} = 5 v, T_A = 25°C

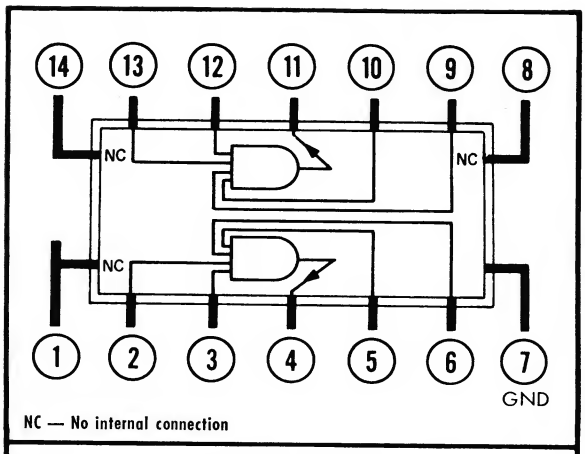
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	27	R_1 = 150 Ω, C_1 = 500 pf	15	40	nsec
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 510 Ω, C_1 = 500 pf	25	80	nsec

† Expander nodes are open unless otherwise noted.

TYPE SN15 933
DUAL 4-INPUT EXPANDER

schematic (each expander)





NC — No internal connection

positive logic

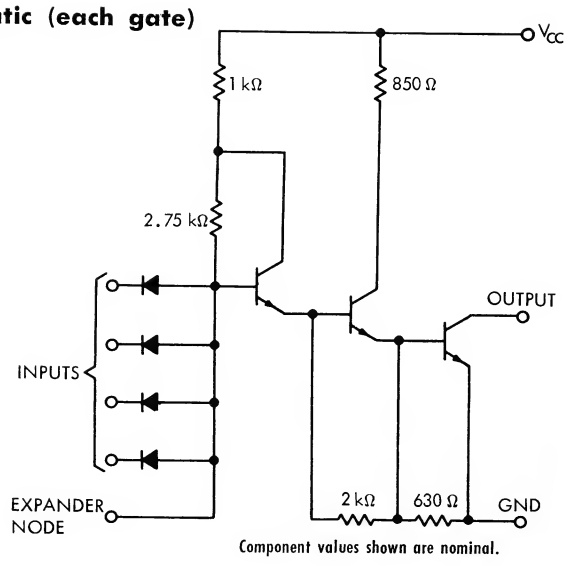
4 = 2•3•5•6 11 = 9•10•12•13

electrical characteristics

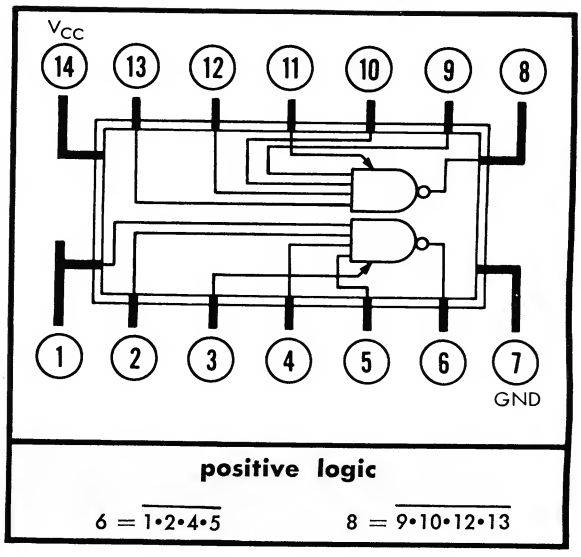
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V_F	Input diode forward voltage	21	I_{out} = 2 ma, T_A = 25°C	0.7	0.82	v
			I_{out} = 2 ma, T_A = –55°C	0.85	0.98	v
			I_{out} = 2 ma, T_A = 125°C	0.5	0.65	v
$I_{in(R)}$	Input diode reverse current	22	V_{in} = 4 v, T_A = 25°C		2	μa
			V_{in} = 4 v, T_A = –55°C		2	μa
			V_{in} = 4 v, T_A = 125°C		5	μa
$I_{out(R)}$	Anode-to-substrate reverse current	23	V_{out} = 4 v, T_A = 25°C and –55°C		10	μa
			V_{out} = 4 v, T_A = 125°C		25	μa

NOTE: A total of four expanders may be connected to an expandable gate to provide a fan-in of 20.

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output 27

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 v, V_{in} = 1.9 v, I_{sink} = 40 ma, T_A = 25°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 2.1 v, I_{sink} = 36 ma, T_A = –55°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 1.7 v, I_{sink} = 36 ma, T_A = 125°C		0.45	v
$V_{out(1)}$	Logical 1 output voltage (off level)	24	V_{CC} = 5.5 v, I_{sink} = 5 ma, T_A = 25°C	6		v
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 25°C and –55°C		–1.6	ma
			V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 125°C		–1.5	ma
$I_{out(1)}$	Output reverse current (off level, worst-case voltage at any input)	25	V_{CC} = 5.5 v, V_{in} = 1.1 v, V_{out} = 4.5 v, T_A = 25°C		100	μa
			V_{CC} = 5.5 v, V_{in} = 1.4 v, V_{out} = 4.5 v, T_A = –55°C		50	μa
			V_{CC} = 5.5 v, V_{in} = 0.8 v, V_{out} = 4.5 v, T_A = 125°C		200	μa
$I_{out(1)}$	Output reverse current (off level, worst-case voltage at expander input)	26	V_{CC} = 5.5 v, $V_{in(X)}$ = 1.8 v, V_{out} = 4.5 v, T_A = 25°C		100	μa
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	V_{CC} = 5 v, T_A = 25°C		20	ma
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	V_{CC} = 8 v, T_A = 25°C		6	ma

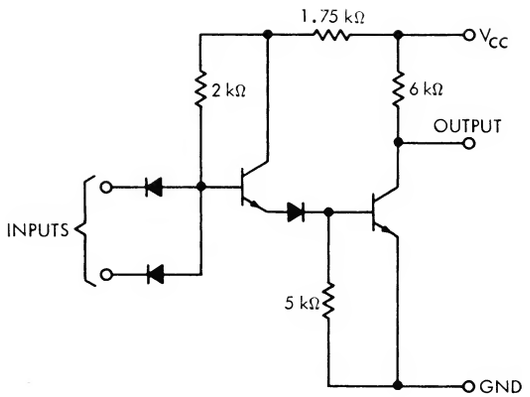
switching characteristics, V_{CC} = 5 v, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	27	R_1 = 150 Ω, C_1 = 100 pf	10	35	nsec
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 510 Ω, C_1 = 20 pf	15	50	nsec

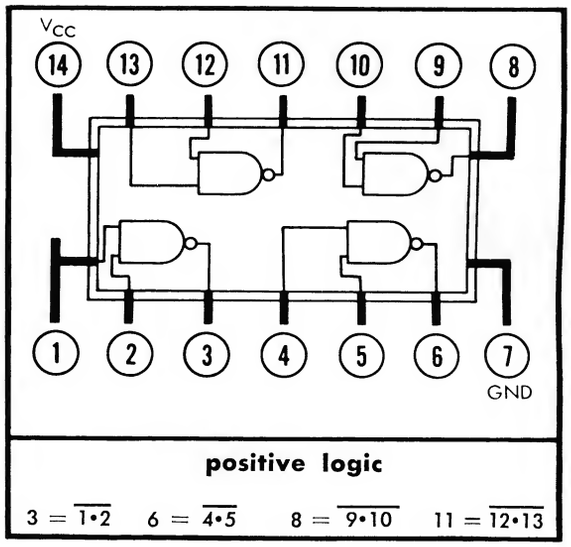
† Expander nodes are open unless otherwise noted.

TYPE SN15 946
QUADRUPLE 2-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$3 = \overline{1 \cdot 2}$ $6 = \overline{4 \cdot 5}$ $8 = \overline{9 \cdot 10}$ $11 = \overline{12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 v, V_{in} = 1.9 v, I_{sink} = 12 ma, T_A = 25°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 2.1 v, I_{sink} = 11.4 ma, T_A = –55°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 1.7 v, I_{sink} = 10.8 ma, T_A = 125°C		0.45	v
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 v, V_{in} = 1.1 v, I_{load} = 0.12 ma, T_A = 25°C	2.6		v
			V_{CC} = 4.5 v, V_{in} = 1.4 v, I_{load} = 0.12 ma, T_A = –55°C	2.5		v
			V_{CC} = 4.5 v, V_{in} = 0.8 v, I_{load} = 0.12 ma, T_A = 125°C	2.5		v

electrical characteristics (continued)

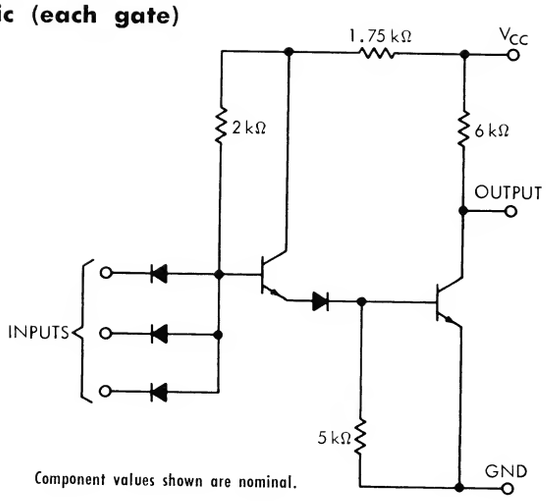
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 25°C and –55°C		–1.6	ma
			V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 125°C		–1.5	ma
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 v, T_A = 25°C		50	μa
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 v, V_{out} = 0, T_A = 25°C	–0.6	–1.34	ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = –55°C		–1.34	ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = 125°C		–1.3	ma
$I_{CC(0)}$	Logical 0 level supply current (all gates)	8	V_{CC} = 5 v, T_A = 25°C		13	ma
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (all gates)	9	V_{CC} = 8 v, T_A = 25°C		11	ma

switching characteristics, V_{CC} = 5 v, T_A = 25°C

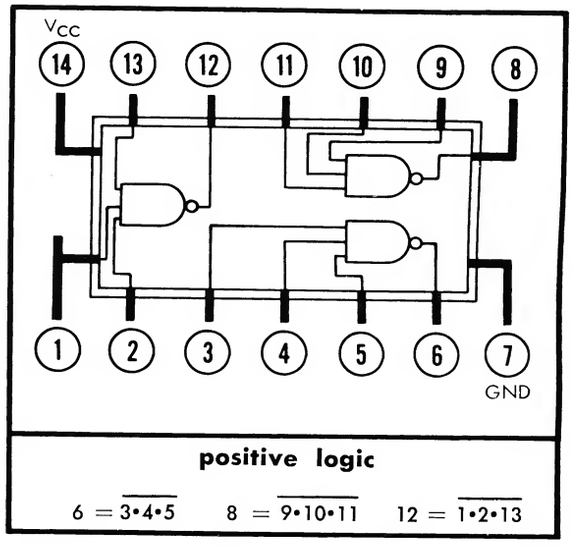
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	27	R_1 = 400 Ω, C_1 = 50 pf	10	30	nsec
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 3.9 kΩ, C_1 = 30 pf	25	80	nsec

TYPE SN15 962
TRIPLE 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{3 \cdot 4 \cdot 5}$ $8 = \overline{9 \cdot 10 \cdot 11}$ $12 = \overline{1 \cdot 2 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 v to 5.5 v

Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 v, V_{in} = 1.9 v, I_{sink} = 12 ma, T_A = 25°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 2.1 v, I_{sink} = 11.4 ma, T_A = –55°C		0.4	v
			V_{CC} = 4.5 v, V_{in} = 1.7 v, I_{sink} = 10.8 ma, T_A = 125°C		0.45	v
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 v, V_{in} = 1.1 v, I_{load} = 0.12 ma, T_A = 25°C	2.6		v
			V_{CC} = 4.5 v, V_{in} = 1.4 v, I_{load} = 0.12 ma, T_A = –55°C	2.5		v
			V_{CC} = 4.5 v, V_{in} = 0.8 v, I_{load} = 0.12 ma, T_A = 125°C	2.5		v

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 25°C and –55°C		2	μa
			V_{CC} = 5.5 v, V_{in} = 4 v, T_A = 125°C		5	μa
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 25°C and –55°C		–1.6	ma
			V_{CC} = 5.5 v, V_{in} = 0, V_R = 4 v, T_A = 125°C		–1.5	ma
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 v, T_A = 25°C		50	μa
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 v, V_{out} = 0, T_A = 25°C	–0.6	–1.34	ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = –55°C		–1.34	ma
			V_{CC} = 5.5 v, V_{out} = 0, T_A = 125°C		–1.3	ma
$I_{CC(0)}$	Logical 0 level supply current (all gates)	8	V_{CC} = 5 v, T_A = 25°C		9.75	ma
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (all gates)	9	V_{CC} = 8 v, T_A = 25°C		8.25	ma

switching characteristics, V_{CC} = 5 v, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	27	R_1 = 400 Ω, C_1 = 50 pf	10	30	nsec
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 3.9 kΩ, C_1 = 30 pf	25	80	nsec

PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

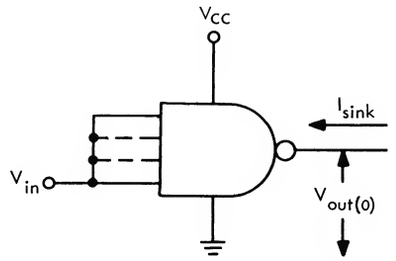
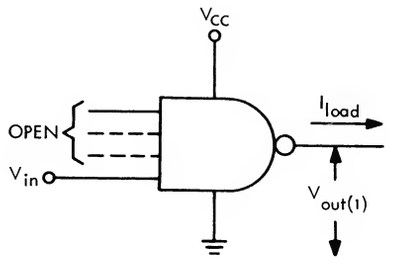


FIGURE 1



1. Each input is tested separately.

FIGURE 2

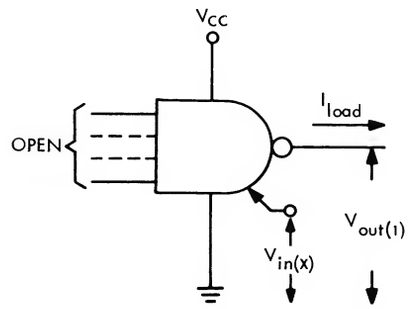
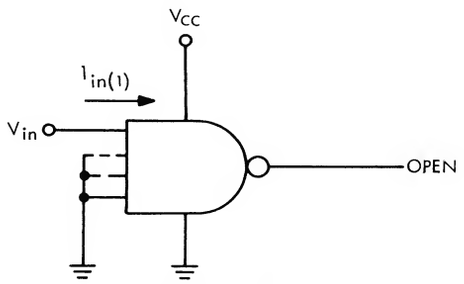
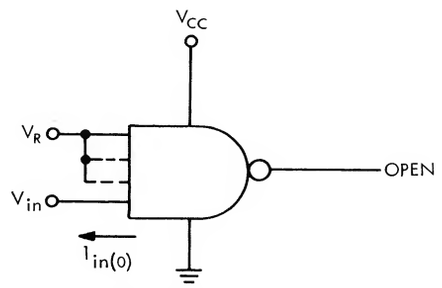


FIGURE 3



1. Each input is tested separately.

FIGURE 4



1. Each input is tested separately.

FIGURE 5

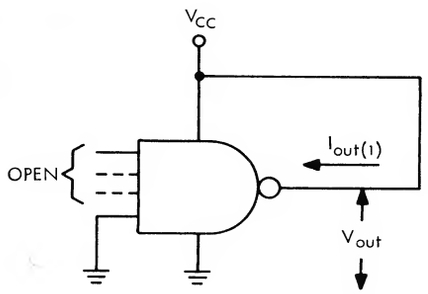


FIGURE 6

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

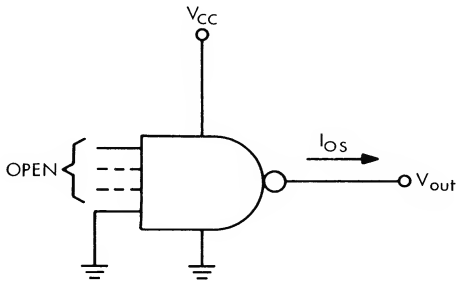


FIGURE 7

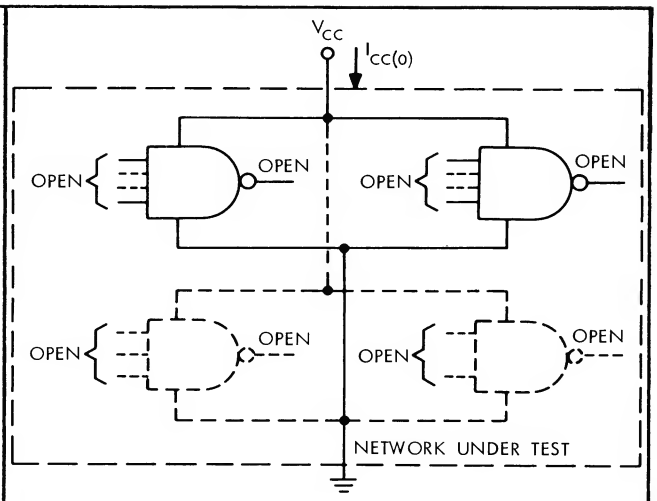


FIGURE 8

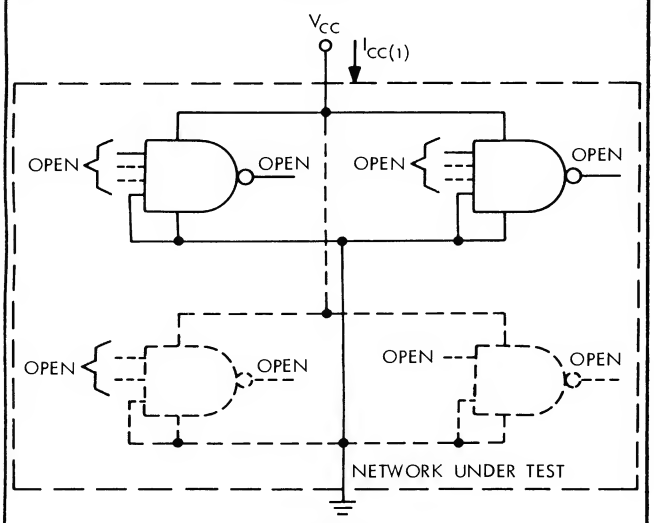
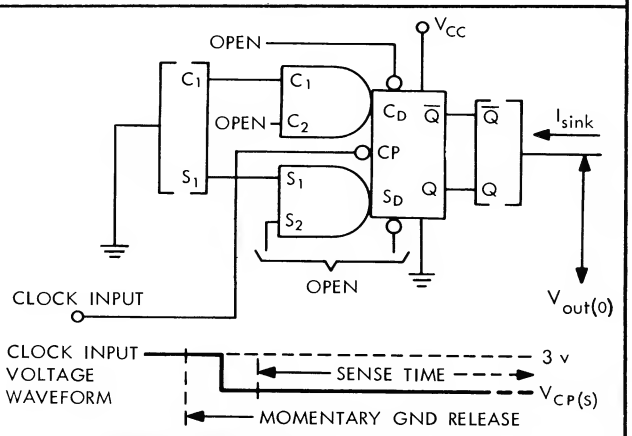
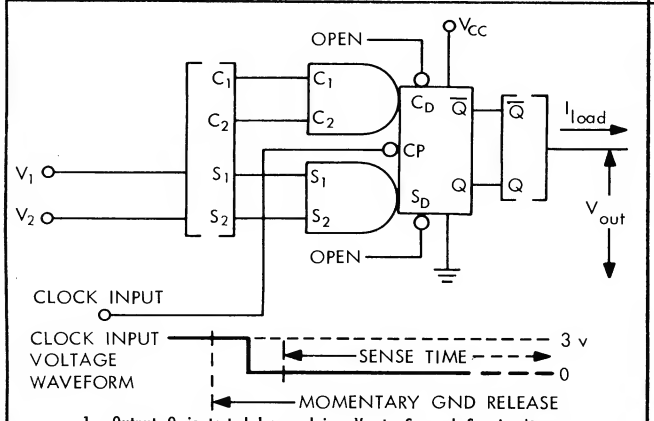


FIGURE 9



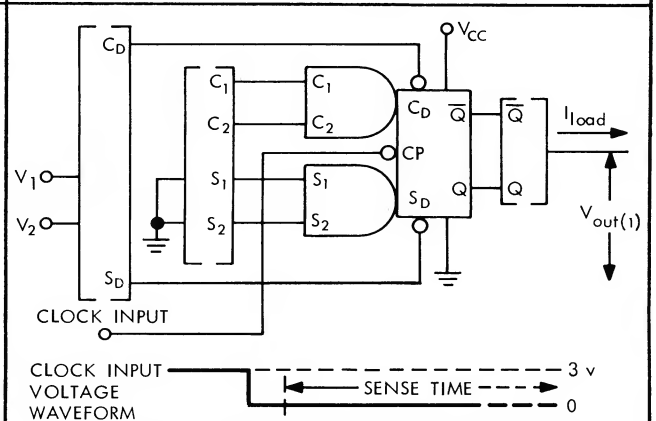
1. Output Q is tested by grounding S_1 and applying a momentary ground to $\overline{Q}$. I_{sink} is driven into Q.
2. Output $\overline{Q}$ is tested by grounding C_1 and applying a momentary ground to Q. I_{sink} is driven into $\overline{Q}$.

FIGURE 10



1. Output Q is tested by applying V_1 to S_1 and S_2 simultaneously, applying V_2 to C_1 and C_2 individually, and loading Q.
2. Output $\overline{Q}$ is tested by applying V_1 to C_1 and C_2 simultaneously, applying V_2 to S_1 and S_2 individually, and loading $\overline{Q}$.
3. Momentary ground is applied to output being tested.

FIGURE 11



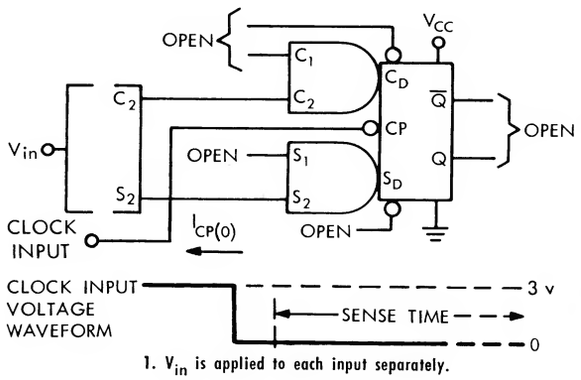
1. Output Q is tested by grounding S_1 and S_2, applying V_1 to C_D and V_2 to S_D, and loading Q.
2. Output $\overline{Q}$ is tested by grounding C_1 and C_2, applying V_1 to S_D and V_2 to C_D, and loading $\overline{Q}$.

FIGURE 12

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. V_{in} is applied to each input separately.

FIGURE 13

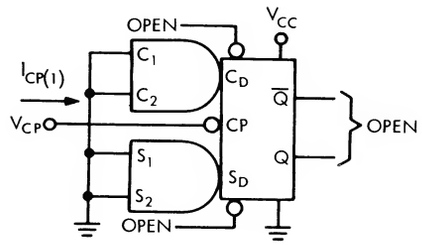
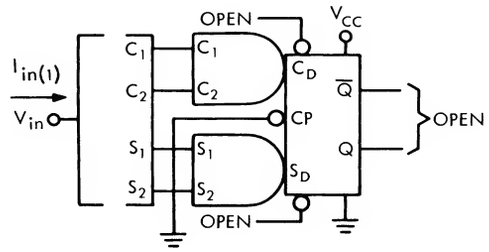
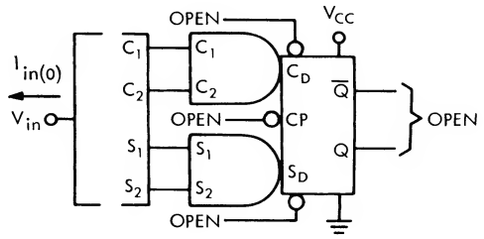


FIGURE 14



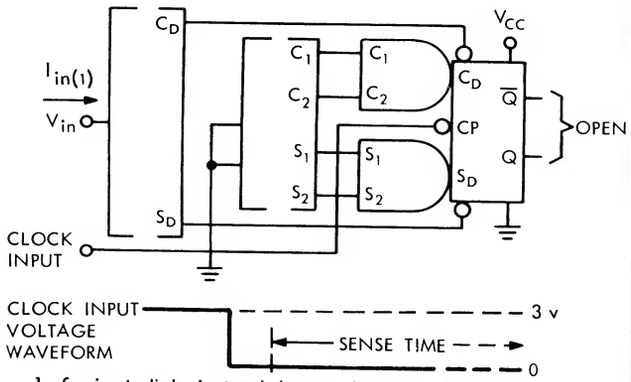
1. V_{in} is applied to each input separately.

FIGURE 15



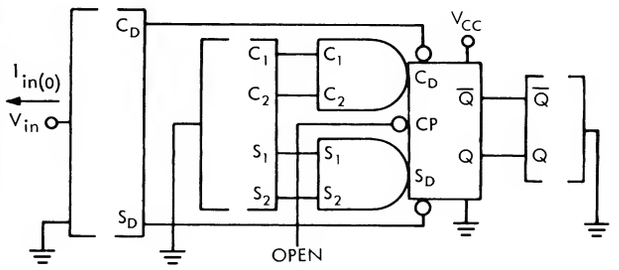
1. V_{in} is applied to each input separately.

FIGURE 16



1. C_D input diode is tested by grounding S_1 and S_2 and applying V_{in} to C_D.
2. S_D input diode is tested by grounding C_1 and C_2 and applying V_{in} to S_D.

FIGURE 17



1. C_D is tested with S_D, S_2 and $\overline{Q}$ grounded.
2. S_D is tested with C_D, C_2 and Q grounded.

FIGURE 18

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

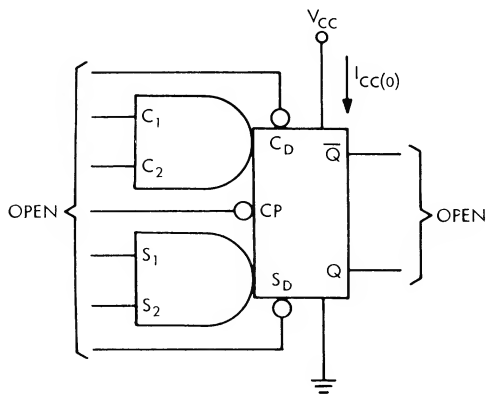


FIGURE 19

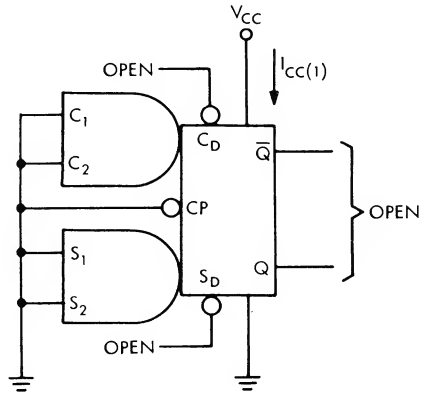
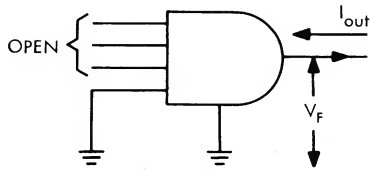
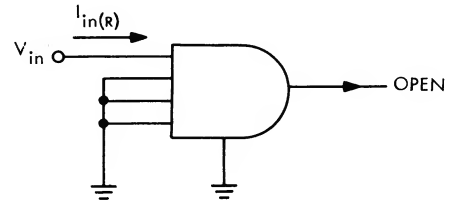


FIGURE 20



1. Each input is tested separately.

FIGURE 21



1. Each input is tested separately.

FIGURE 22

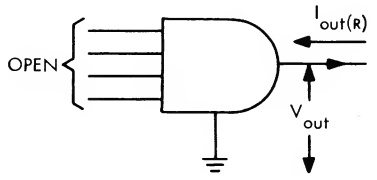


FIGURE 23

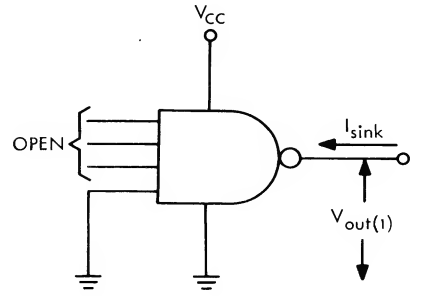
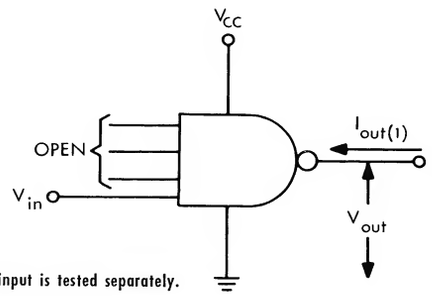


FIGURE 24

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)



1. Each input is tested separately.

FIGURE 25

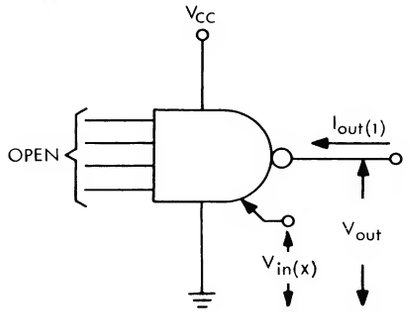
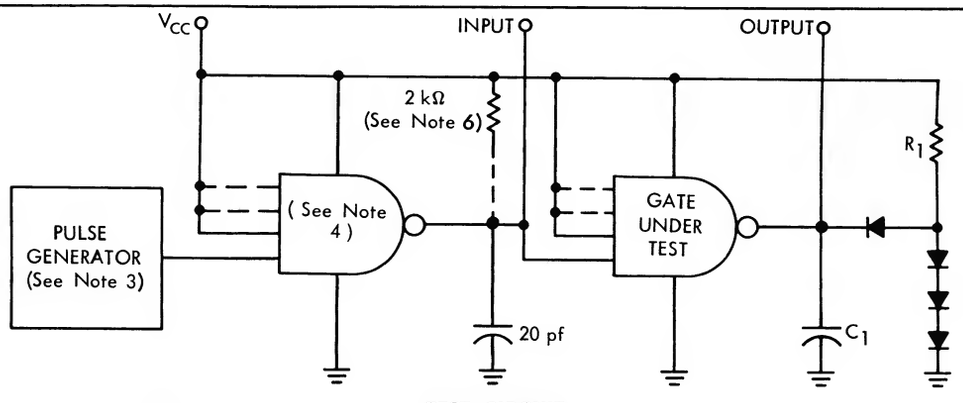


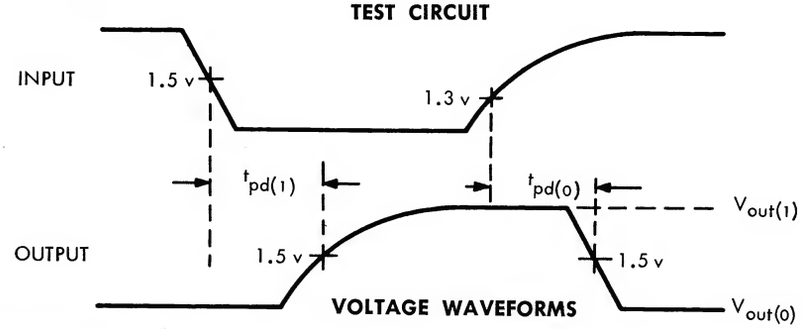
FIGURE 26

† Arrows indicate actual direction of current flow.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Each gate is tested separately.

2. All diodes are 1N916.

3. The generator has the following characteristics:
$V_{out} = 3$ v, $t_r \leq 15$ nsec, $t_f \leq 15$ nsec, $t_p = 300$ nsec, PRR = 1 Mc, $Z_{out} \cong 50\ \Omega$.

4. The driving network is of the same type as the gate under test.

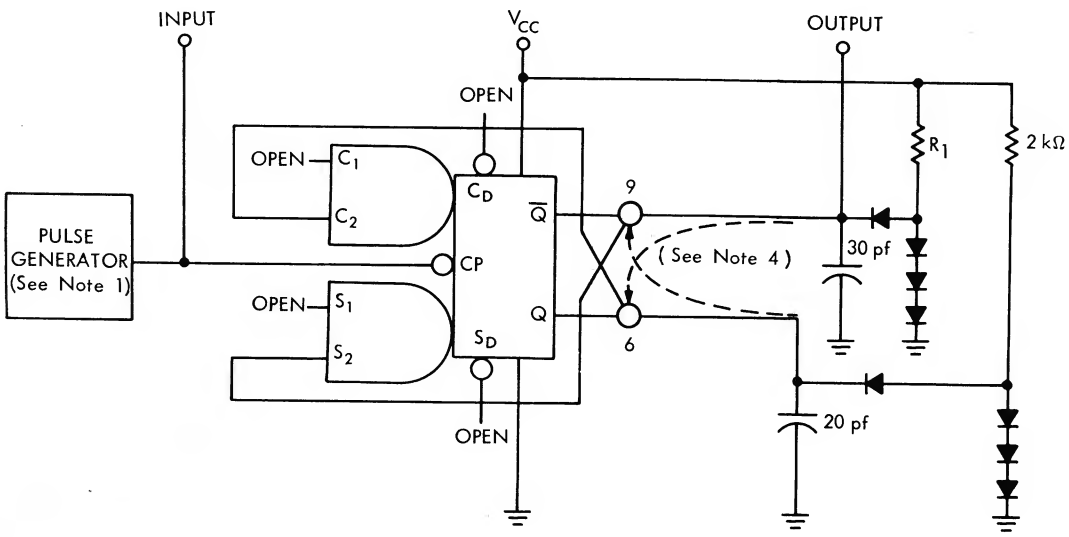
5. Voltage values are with respect to network ground terminal.

6. When testing the SN15 944, connect the 2 kΩ resistor as shown, omit all diodes, and connect resistor R_1 to capacitor C_1 and output.

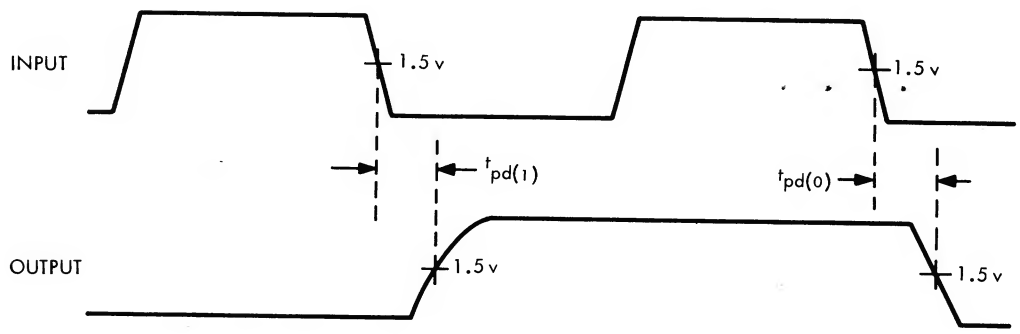
FIGURE 27 — GATE PROPAGATION DELAY

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
$V_{out} = 3$ v, $t_r \leq 15$ nsec, $t_f \leq 15$ nsec, $t_p = 300$ nsec, PRR = 1 Mc, $Z_{out} \simeq 50\ \Omega$.
2. All diodes are 1N916.
3. Voltage values are with respect to network ground terminal.
4. Test circuit shows loading when output $\overline{Q}$ is tested. When output Q is tested, loading is interchanged as indicated by the dotted lines.

FIGURE 28 — FLIP-FLOP PROPAGATION DELAY

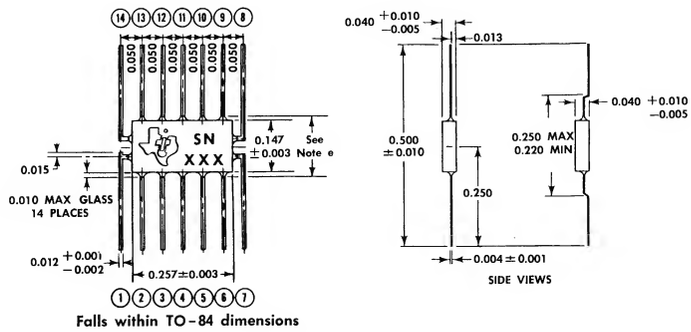
SERIES 15 930
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

MECHANICAL DATA

general

SOLID CIRCUIT semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 15 930 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pack carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE

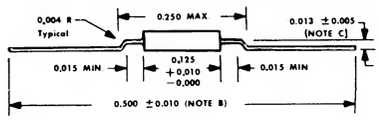


NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Overall dimensions of package and glass meniscus can be held to 0.155 by special request.

leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.185 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.185 inches.

FORMED LEADS



NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

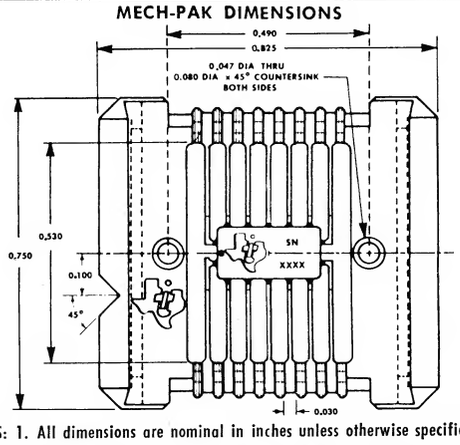
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inches thick and has an insulation resistance of 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.185 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	−6	−7	−1	−2	−3	−4	−5

†Patented by Texas Instruments Incorporated.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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SEMICONDUCTOR-COMPONENTS DIVISION
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